

<b>Notice of References Cited</b>		Application/Control No.	Applicant(s)/Patent Under Reexamination LAMPAERT ET AL.	
		Examiner Leigh Marie Garbowski	Art Unit 2825	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
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	C	US-			
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**FOREIGN PATENT DOCUMENTS**

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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
*	U	J.D. CONWAY et al., "An Automatic Layout Generator for Analog Circuits," 1992 IEEE, pages 513-519.
*	V	M. DESSOUKY et al., "Layout-Oriented Synthesis of High Performance Analog Circuits," ACM 2000, pages 53-57.
*	W	J.A. PRIETO et al., "A Performance-Driven Placement Algorithm with Simultaneous Place&Route Optimization for Analog IC's," 1997 IEEE, pages 389-394.
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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